ABSTRACT

An improved technique and associated apparatus for timing calibration of a logic device is provided. A calibration test pattern is transferred to a logic device first at a data rate slower than normal operating speed to ensure correct capture of the pattern at the device to be calibrated. Once the pattern is correctly captured and stored, the test pattern is transmitted to the logic device at the normal operating data rate to perform timing calibration. The improved technique and apparatus permits the use of any pattern of bits as a calibration test pattern, programmable by the user or using easily-interchangeable hardware.